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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,656	10/07/2004	Hui Wang	495152001000	9021

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Hui "David" Wang, President
ACM RESEARCH, INC.
4378 Enterprise Street
Fremont, CA 94538

EXAMINER	
YAKULIS, JEFFREY C	
ART UNIT	**PAPER NUMBER**
1753	

MAIL DATE	DELIVERY MODE
07/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/510,656	WANG ET AL.	
	Examiner	Art Unit	
	Jeff Yakulis	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/7/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/29/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Provisional documents directed to Wang et al., Yao et al., and both international searched reports were considered but lined through because they are not prior art references available to the public and will be excluded from the patent if it would happen to issue.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 7-8, 13-15, and 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Reid et al. (6,793,796).

Regarding claim 1 and 2, Reid et al. teaches electroplating with a first current density in the range of 0.2-5 mA/cm2 during an initiation phase prior to recessed features being filled providing for a thin continuous conducting surface extending over the field and recessed regions of the substrate (col. 5 lines 45-67 and col. 6 lines 1-16). Reid et al further teaches a bottom up filling phase where trenches and vias are substantially filled from the bottom of the feature upwards using current densities ranging from about 0.2-5 mA/cm2 specifically, 3 mA/cm2 (example 2) and gradually

increasing over time to about 4-45 mA/cm2 specifically, 10 mA/cm2 (example 2) until all the recessed features have aspect ratios of less than about 0.5 (aspect ratios of less than 0.5 would encompass features with aspect ratios of 0 or essentially planar, col. 6 lines 18-34 and col. 6 lines 55-61, see also figure 1).

Regarding claim 3, Reid et al teaches the current density during the initiation phase or first current density can be constant (col. 5 lines 66-67).

Regarding claim 4, Reid et al. teaches the current density during the initiation phase or first current density can be ramped or increase (col. 5 lines 62-67, col. 6 lines 1-4).

Regarding claim 7, Reid et al. teaches applying a first current density during an initiation phase, which can be pulsed implying the increase and decreasing of the current (col. 5 lines 66-67 and col. 6 lines 1-6).

Regarding claim 8, Reid et al. teaches electroplating with a second current density during a bottom up filling phase at a constant rate of 10 mA/cm2 for 30 seconds (col. 8 lines 43-44).

Regarding claim 13, Reid et al. teaches electroplating onto a surface having features with a range of different aspect ratios/densities (col. 2 lines 51-53). Reid et al. further teaches a bottom up filling phase filling recesses with high aspect ratios until all recesses have about an aspect ratio of 0.5 or less, encompassing planarized recesses or aspect ratios of 0 (col. 6 lines 18-34 and col. 6 lines 55-61). Reid et al. finally teaches a low aspect ratio filling phases where all recesses having high aspect ratios have been either filled converted to a low aspect ratio and essentially a final layer of metal is

deposited over the filled and unfilled recesses on the order of a 0.7-14 micrometers (col. 6 lines 55-61 and col. 7 lines 1-2, See also for example figure 1 for recesses having multiple densities as well as table 3 and 4).

Regarding claim 14, Reid et al. further discloses a final stage in plating of the wafer called the low aspect ratio filling phase, which in order to maximize throughput during processing the maximum possible current is applied usually on the range of 15-75 mA/cm2, typically from about 20-50 mA/cm2, and most typically from about 25-40 mA/cm2 (col. 6 lines 63-68 and col. 7 lines 1-8, see example one showing three increasing current steps being applied). Reid et al. further teaches multiple recesses of different sizes being plated (col. 2 lines 51-53 and table 3 and 4). Reid et al. further discloses the third current density or low aspect ratio begins when features have either been converted to low aspect ratios or have been filled showing the realization that one or multiple recesses of increasing density/size can be filled during the onset of the third current range/low aspect ratio filling phase (col. 6 lines 63-67 and col. 7 lines 1-9).

Regarding claim 15, Reid et al. teaches the electrolyte fluid containing an accelerator, suppressor, and leveler (col. 4 lines 7-9).

Regarding claim 17, Reid et al. teaches controlling the grain size of the metal layer with additives in the electrolyte fluid (col. 4 lines 13-17).

Regarding claim 18, Reid et al. teaches additives including a brightener and accelerator (col. 4 lines 10-25).

micrometers for the width between recesses [14,16] (figure 1, table 3 and 4). In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reid et al (6,793,796) as applied to claim 1 above, and further in view of Mayer et al. (6,946,065).

Reid et al. teaches all the elements of claim 1 and a second current density range (col. 6 lines 18-35) but fails to disclose: decreasing the current density.

Mayer et al. is directed toward electroplating metal into microscopic recessed features using a bottom up-filling method to prevent the introduction of voids formed in the plated layer (abstract). Mayer et al. teaches the current being applied to a wafer during deposition is generally selected based on feature density as well as the aspect ratio of the feature sizes and will vary considerably from case to case, wafer type to wafer type depending on the characteristics of the features present (col. 3 lines 22-42). Mayer et al. further teaches that applied current relates to the consumption of the additives present in the electrolyte and ultimately the rate at which ions were deposited onto the substrate (col. 17 lines 13-41). Mayer et al. further teaches applied current effects the rate at which additives are used and that applying a substantially small current depletes recesses having large aspect ratios thus allowing for a controlled deposition in these areas initially (col. 17 lines 13-41)

Claim Rejections - 35 USC § 103

4. Claims 5-6, 9-10, and 12 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Reid et al. (6,793,796).

Regarding claim 5 and 6, Reid et al. teaches ramping the current during the initiation phase or first current density. It is either inherent that the increase is linear or nonlinear to choose such an increase as the increase must be one of linear or non-linear. Ramping such a current during the entire initiation phase would allow for a linear increase in current (col. 5 lines 62-65). Reid et al teaches ramping the current density during the end of the initiation phase providing for a constant initial current than gradually increasing it at the end of the phase, which would thus provide for a non-linear profile (col. 5 lines 62-65).

Regarding claim 9 and 10, Reid et al. teaches electroplating using a second current density during a bottom up filling phase increasing over a period of time and discussing a set pattern for the increase implying a non-linear increase (col. 6 lines 55-61). It is either inherent that the increase is linear or nonlinear to choose such an increase as the increase must be one of linear or non-linear.

Regarding claim 12, Reid et al. teaches electroplating a metal onto a surface with recessed features with a having a range between 0.15 micro-meters to 1.7 micro-meters (col. 2 lines 51-53, figure 1, and table 3 and 4). Reid et al. further teaches spacing of about 0.45 micrometer based on the width between recess [14] and recess [16] being three times the width of recess [14] and applying the minimum feature size given in table 3 and 4 (0.15 micrometers) one can arrive at a value of around 0.45

It would have been obvious to decrease the current during electroplating of a metal layer onto substrate because current applied during electroplating is a result effective variable capable of optimization. One having ordinary skill in the art at the time the invention was made would know to increase or decrease the current based on the teachings of Mayer et al. and apply it to the three step plating method taught by Reid et al. depending on how fast the deposition rate needed to be and further based upon the feature sizes and densities (MPEP 2144.05 optimization of ranges).

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reid et al. (6,793,796).

Regarding claim 12, Reid et al. teaches electroplating a metal onto a surface with recessed features with a having a range between 0.15 micro-meters to 1.7 micro-meters (col. 2 lines 51-53, figure 1, and table 3 and 4). Reid et al. further teaches spacing of about 0.45 micrometer based on the width between recess [14] and recess [16] being three times the width of recess [14] and applying the minimum feature size given in table 3 and 4 (0.15 micrometers) one can arrive at a value of around 0.45 micrometers for the width between recesses [14,16] (figure 1, table 3 and 4).

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reid et al. (6,793,796).

Regarding claim 16, Reid et al. teaches a leveler having a concentration of 0.5-8 ml/l, an accelerator concentration 0.5-8 ml/l, and a suppressor concentration of 1-6 ml/l. Reid et al. fails to disclose a suppressor concentration within the range of 7-9 ml/l.

Reid et al. however does teach pitting observed on the wafer surface is dependent upon the concentration of the suppressing agent, its molecular weight, and whether it is hydrophobic or hydrophilic (table 6, col. 9 lines 45-48 and col. 10 lines 55-61).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to adjust the concentration level of the suppressor to a desired ranged based on observed pitting in the wafer and one having ordinary skill would know to adjust the concentration in such a way to minimize pitting on the plated surface (MPEP 2144.05 optimization of ranges).

7. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reid et al. (6,793,796) as applied to claim 1 above, and further in view of Basol et al. (6,610,190).

Regarding claim 19 and 20, Reid et al teaches all the elements of claim 1 mentioned above but fails to disclose: rotating the semiconductor structure with a rotation speed of 50-200 RPM or specifically 125 RPM.

Basol et al. is directed toward depositing a material onto the surface of semi-conductor wafer (abstract). Basol et al. teaches rotating a wafer at a speed of 1-250 rpm (col. 13 lines 15-16). Basol et al. teaches that by rotating the wafer, non-uniformities in the deposited later can be minimized allowing for a more uniform coating (col. 13 lines 24-26).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to rotate the wafer as done by Basol et al. and use it in the

electroplating method discussed by Reid et al. as it would allow for a much more uniform coating later to be deposited onto the seed layer.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dubin (2002/0074234, 6,432,8221, and 6,893,550) and Basol (6,858,121).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Yakulis whose telephone number is 571-272-9807. The examiner can normally be reached on M-F 9:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexa Neckel can be reached on 571-272-1446. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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JCY

ALEXA D. NECKEL
SUPERVISORY PATENT EXAMINER